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| **Week** | **Dates** | **Tasks** |
| 1 | 10/13 – 10/19 | (1) Submit preliminary proposal |
| 2 | 10/20 – 10/26 | (1) Submit full proposal |
| 3 | 10/27 – 11/2 | (1) Research implementation strategies for main blocks  (2) Write pseudo-code for main blocks  (3) Prepare design review |
| 4 | 11/3 – 11/9 | (1) Present design review  (2) Begin Verilog development of main functional blocks |
| 5 | 11/10 – 11/16 | (1) Complete Verilog development of main functional blocks  (2) Begin testing of main blocks |
| 6 | 11/17 – 11/23 | (1) Complete testing of main functional blocks  (2) Begin Verilog development of top-level module  (3) Complete development of top-level module  (4) Begin testing of top-level module |
| 7 | 11/24 – 11/30 | (1) Complete testing of top-level Verilog module  (2) Prepare final presentation and demonstration  (3) Complete final report |
| 8 | 12/1 – 12/7 | (1) Final presentation  (2) Demonstration  (3) Submit final report |

Oluwatosin Adeosun:

(1) Gaussian image smoothing – Verilog development and testing

(2) Top-level module – Testing

(3) Group documents/presentations – Contributor

Sukhyun Hong:

(1) Directional non-maximal suppression – Verilog development and testing

(2) Top-level module – Verilog development

(3) Group documents/presentations – Contributor

Eric Nielsen:

(1) Threshold calculation & hysteresis thresholding – Verilog development and testing

(2) Top-level module – Testing

(3) Group documents/presentations – Contributor

(4) Monitoring progress and negotiating task distribution

Jiyuan Zhao:

(1) Gradient & magnitude calculation – Verilog development and testing

(2) Top-level module – Verilog development

(3) Group documents/presentations – Contributor

**Fixed Success Criteria**

1. (2 points) Test benches exist for all top-level components and the entire design. The test benches for the entire design can be demonstrated or documented to cover all of the functional requirements given in the design specific success criteria.
2. (4 points) Entire design synthesizes completely, without any inferred latches, timing arcs, and, sensitivity list warnings.
3. (2 points) Source and mapped version of the complete design behave the same for all test cases. The mapped version simulates without timing errors except at time zero.
4. (2 points) A complete IC layout is produced that passes all geometry and connectivity checks.
5. (2 points) The entire design complies with targets for area, pin count, throughput (if applicable), and clock rate. The final targets for these parameters will be determined by course staff based on your design review. Failure to reach any of the targets will result a score of 1 out of 2 provided that you are within 50% on area, 10% on pin count, and 25% on throughput. Doing worse in any category will result in a score of 0 out of 2.

**Design Specific Success Criteria**

1. (1 points) Demonstrate by simulation of a Verilog test bench that the complete design is able to produce a smoothed image following the Gaussian block.
2. (1 points) Demonstrate by simulation of a Verilog test bench that the complete design is able to add a 1-pixel border to the smoothed image coming from the Gaussian block.
3. (1 points) Demonstrate by simulation of Verilog test benches that the complete design is able to accurately calculate gradients and magnitudes of the smoothed, bordered image.
4. (1 points) Demonstrate by simulation of Verilog test benches that the complete design is able to produce an image with thinned edges following the suppression block.
5. (4 points) Demonstrate by simulation of Verilog test benches that the complete design is able to produce a bitmap image with edges accurately detected as the output of the overall design.